TEXAS INSTRUMENTS

LMZ14201H

1A SIMPLE SWITCHER Power Module for High Output Voltage

Easy to use 7 pin package

Top View Bottom View

30135430

TO-PMOD 7 Pin Package
10.16 x 13.77 x 4.57 mm (0.4 x 0.542 x 0.18 in)
θ_{JA} = 16°C/W, θ_{JC} = 1.9°C/W
RoHS Compliant

Electrical Specifications

- Up to 1A output current
- Input voltage range 6V to 42V
- Output voltage as low as 5V
- Efficiency up to 97%

Key Features

- Integrated shielded inductor
- Simple PCB layout
- Flexible startup sequencing using external soft-start and precision enable
- Protection against inrush currents
- Input UVLO and output short circuit protection
- – 40°C to 125°C junction temperature range
- Single exposed pad and standard pinout for easy mounting and manufacturing
- Low output voltage ripple
- Pin-to-pin compatible family:
  LMZ14203H/2H/1H (42V max 3A, 2A, 1A)
  LMZ14203/2/1 (42V max 3A, 2A, 1A)
  LMZ12003/2/1 (20V max 3A, 2A, 1A)
- Fully enabled for Webench® Power Designer

Applications

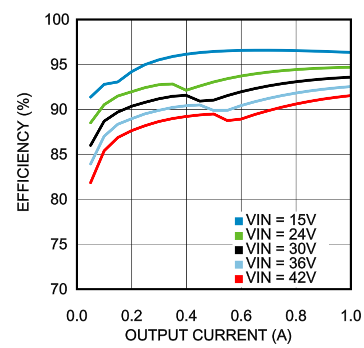
- Intermediate bus conversions to 12V and 24V rail
- Time critical projects
- Space constrained / high thermal requirement applications
- Negative output voltage applications

Performance Benefits

- High efficiency reduces system heat generation
- Low radiated EMI (EN 55022 Class B compliant) (*Note 5*)
- No compensation required
- Low package thermal resistance

System Performance

Efficiency V_{OUT} = 12V



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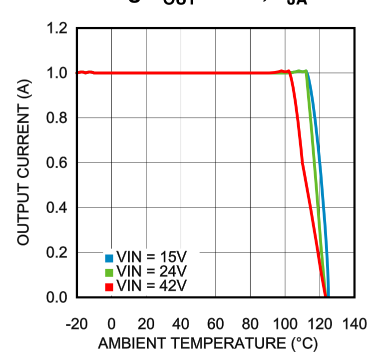
Thermal Derating V_{OUT} = 12V, θ_{JA} = 16°C/W



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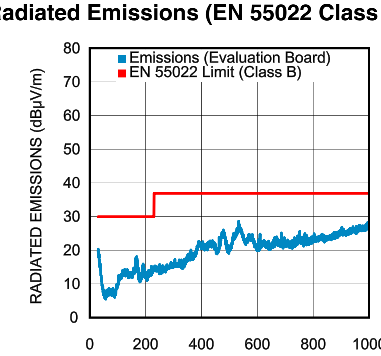
Radiated Emissions (EN 55022 Class B)



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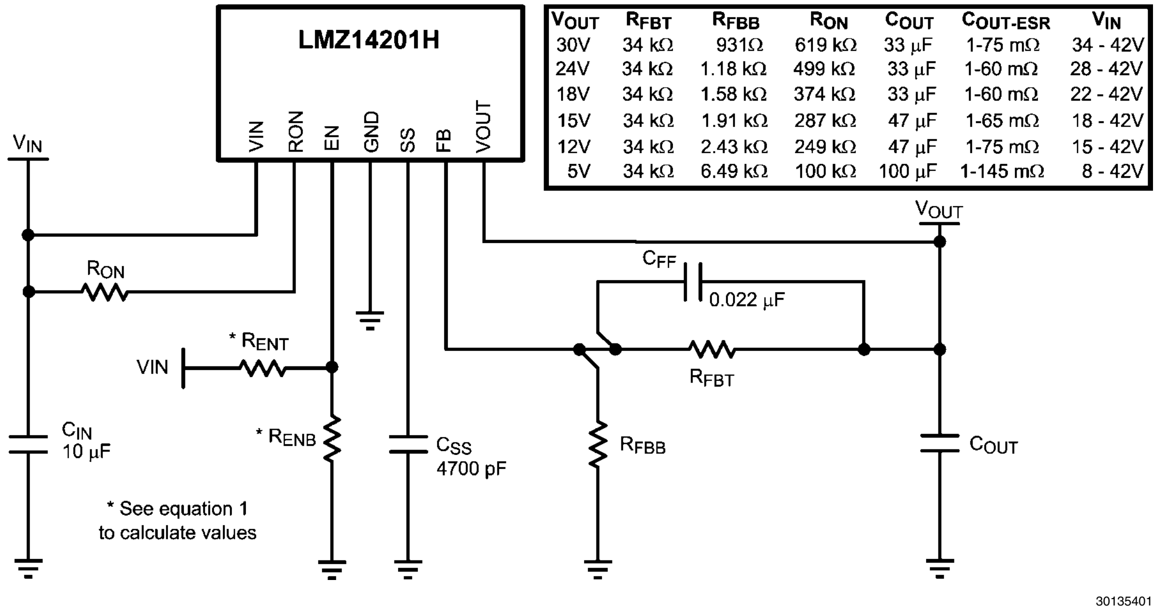
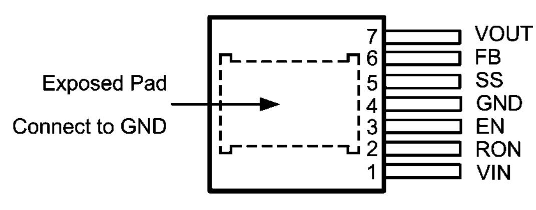
Simplified Application Schematic



V_{OUT}	R_{FBT}	R_{FBB}	R_{ON}	C_{OUT}	$C_{OUT\text{-}ESR}$	V_{IN}
30V	34 kΩ	931Ω	619 kΩ	33 µF	1-75 mΩ	34 - 42V
24V	34 kΩ	1.18 kΩ	499 kΩ	33 µF	1-60 mΩ	28 - 42V
18V	34 kΩ	1.58 kΩ	374 kΩ	33 µF	1-60 mΩ	22 - 42V
15V	34 kΩ	1.91 kΩ	287 kΩ	47 µF	1-65 mΩ	18 - 42V
12V	34 kΩ	2.43 kΩ	249 kΩ	47 µF	1-75 mΩ	15 - 42V
5V	34 kΩ	6.49 kΩ	100 kΩ	100 µF	1-145 mΩ	8 - 42V

Connection Diagram



Top View
7-Lead TO-PMOD

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LMZ14201HTZ	TO-PMOD-7	TZA07A	250 Units on Tape and Reel
LMZ14201HTZX	TO-PMOD-7	TZA07A	500 Units on Tape and Reel
LMZ14201HTZE	TO-PMOD-7	TZA07A	45 Units in a Rail

Pin Descriptions

Pin	Name	Description
1	VIN	Supply input — Additional external input capacitance is required between this pin and the exposed pad (EP).
2	RON	On time resistor — An external resistor from V_{IN} to this pin sets the on-time and frequency of the application. Typical values range from 100k to 700k ohms.
3	EN	Enable — Input to the precision enable comparator. Rising threshold is 1.18V.
4	GND	Ground — Reference point for all stated voltages. Must be externally connected to EP.
5	SS	Soft-Start — An internal 8 µA current source charges an external capacitor to produce the soft-start function.
6	FB	Feedback — Internally connected to the regulation, over-voltage, and short-circuit comparators. The regulation reference point is 0.8V at this input pin. Connect the feedback resistor divider between the output and ground to set the output voltage.
7	VOUT	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and the EP.
EP	EP	Exposed Pad — Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

VIN, RON to GND	-0.3V to 43.5V
EN, FB, SS to GND	-0.3V to 7V
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
ESD Susceptibility(Note 2)	± 2 kV
Peak Reflow Case Temperature (30 sec)	245°C

For soldering specifications, refer to the following document: www.ti.com/lit/snoa549c

Operating Ratings (Note 1)

V_{IN}	6V to 42V
EN	0V to 6.5V
Operation Junction Temperature	−40°C to 125°C

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24V, V_{OUT} = 12V, R_{ON} = 249kΩ

Symbol	Parameter	Conditions	Min (Note 3)	Typ (Note 4)	Max (Note 3)	Units
SYSTEM PARAMETERS						
Enable Control						
V_{EN}	EN threshold trip point	V_{EN} rising	**1.10**	1.18	**1.25**	V
V_{EN-HYS}	EN threshold hysteresis			90		mV
Soft-Start						
I_{SS}	SS source current	V_{SS} = 0V	**8**	10	**15**	µA
I_{SS-DIS}	SS discharge current			-200		µA
Current Limit						
I_{CL}	Current limit threshold	DC average	**1.5**	1.95	**2.7**	A
VIN UVLO						
VIN_{UVLO}	Input UVLO	EN pin floating V_{IN} rising		3.75		V
$VIN_{UVLO-HYST}$	Hysteresis	EN pin floating V_{IN} falling		130		mV
ON/OFF Timer						
t_{ON-MIN}	ON timer minimum pulse width			150		ns
t_{OFF}	OFF timer pulse width			260		ns
Regulation and Over-Voltage Comparator						
V_{FB}	In-regulation feedback voltage	V_{IN} = 24V, V_{OUT} = 12V V_{SS} >+ 0.8V T_J = -40°C to 125°C I_{OUT} = 10mA to 1A	**0.782**	0.803	**0.822**	V
		V_{IN} = 24V, V_{OUT} = 12V V_{SS} >+ 0.8V T_J = 25°C I_{OUT} = 10mA to 1A	0.786	0.803	0.818	V

Symbol	Parameter	Conditions	Min (Note 3)	Typ (Note 4)	Max (Note 3)	Units
V_{FB}	In-regulation feedback voltage	V_{IN} = 36V, V_{OUT} = 24V V_{SS} >+ 0.8V T_J = -40°C to 125°C I_{OUT} = 10mA to 1A	**0.780**	0.803	**0.823**	V
		V_{IN} = 36V, V_{OUT} = 24V V_{SS} >+ 0.8V T_J = 25°C I_{OUT} = 10mA to 1A	0.787	0.803	0.819	V
$V_{FB\text{-}OVP}$	Feedback over-voltage protection threshold			0.92		V
I_{FB}	Feedback input bias current			5		nA
I_Q	Non Switching Input Current	V_{FB}= 0.86V		1		mA
I_{SD}	Shut Down Quiescent Current	V_{EN}= 0V		25		μA
Thermal Characteristics						
T_{SD}	Thermal Shutdown	Rising		165		°C
$T_{SD\text{-}HYST}$	Thermal Shutdown Hysteresis			15		°C
θ_{JA}	Junction to Ambient	4 layer Printed Circuit Board, 7.62cm x 7.62cm (3in x 3in) area, 1 oz Copper, No air flow		16		°C/W
		4 layer Printed Circuit Board, 6.35cm x 6.35cm (2.5in x 2.5in) area, 1 oz Copper, No air flow		18.4		°C/W
θ_{JC}	Junction to Case	No air flow		1.9		°C/W
PERFORMANCE PARAMETERS						
ΔV_{OUT}	Output Voltage Ripple	V_{OUT} = 5V, C_{OUT} = 100μF 6.3V X7R		8		mV_{PP}
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 16V to 42V, I_{OUT}= 1A		.01		%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = 24V, I_{OUT}= 0A to 1A		1.5		mV/A
η	Efficiency	V_{IN} = 24V V_{OUT} = 12V I_{OUT} = 0.5A		94		%
η	Efficiency	V_{IN} = 24V V_{OUT} = 12V I_{OUT} = 1A		92		%

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

Note 3: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

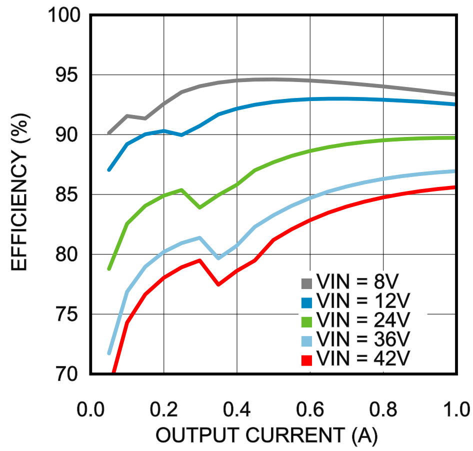
Note 4: Typical numbers are at 25°C and represent the most likely parametric norm.

Note 5: EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007.

Typical Performance Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 24V; Cin = 10uF X7R Ceramic; C_O = 47uF; T_{AMB} = 25°C.

Efficiency V_{OUT} = 5.0V T_{AMB} = 25°C



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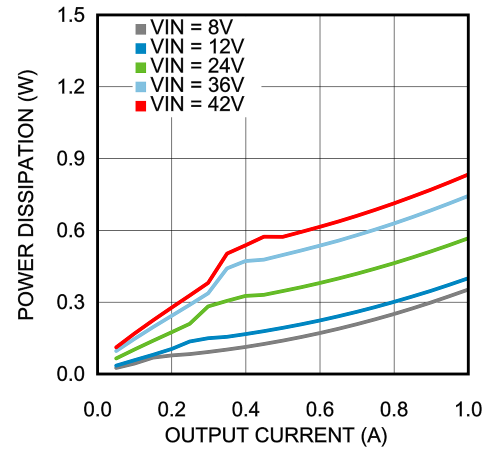
Power Dissipation V_{OUT} = 5.0V T_{AMB} = 25°C



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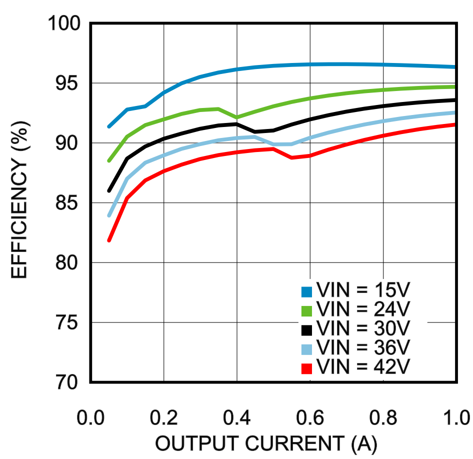
Efficiency V_{OUT} = 12V T_{AMB} = 25°C



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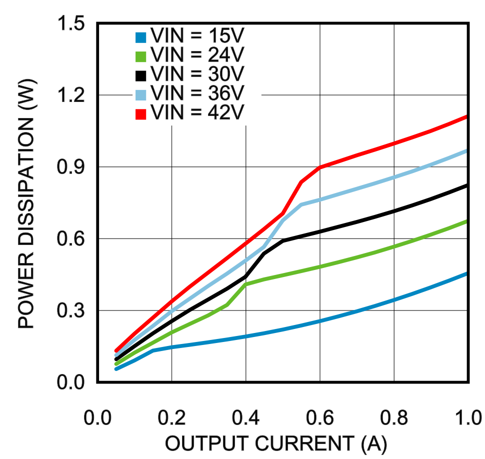
Power Dissipation V_{OUT} = 12V T_{AMB} = 25°C



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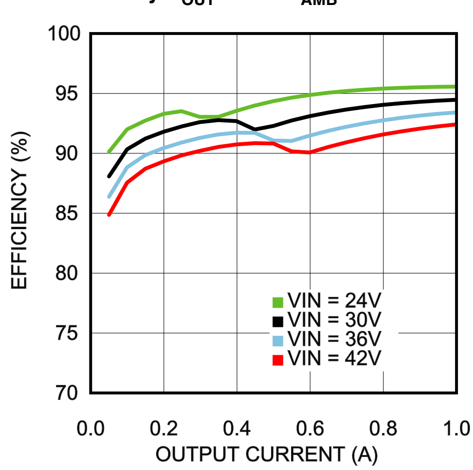
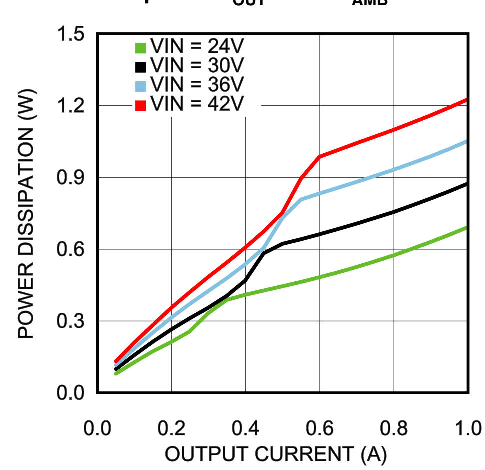
Efficiency V_{OUT} = 15V T_{AMB} = 25°C



30135409

Power Dissipation V_{OUT} = 15V T_{AMB} = 25°C



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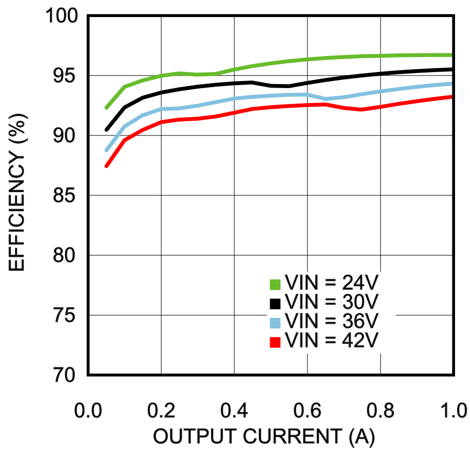
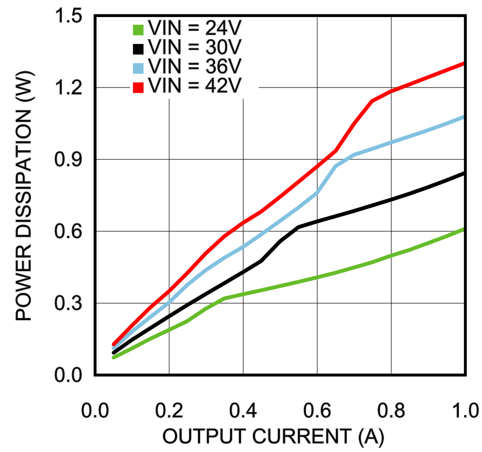
Efficiency V_{OUT} = 18V T_{AMB} = 25°C



30135449

Power Dissipation V_{OUT} = 18V T_{AMB} = 25°C



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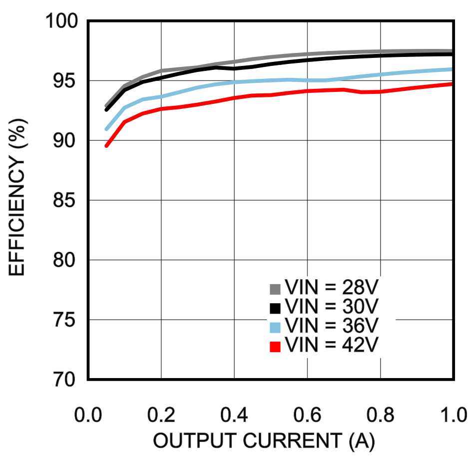
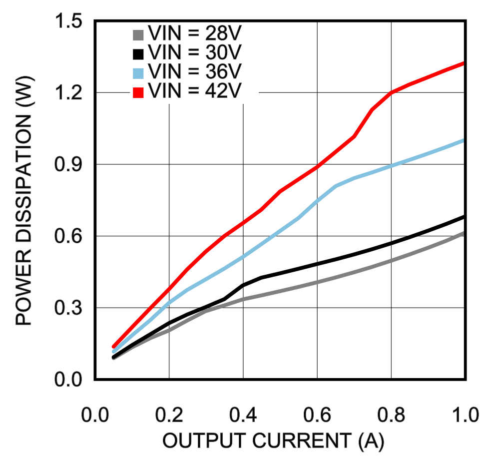
Efficiency V_{OUT} = 24V T_{AMB} = 25°C



30135447

Power Dissipation V_{OUT} = 24V T_{AMB} = 25°C



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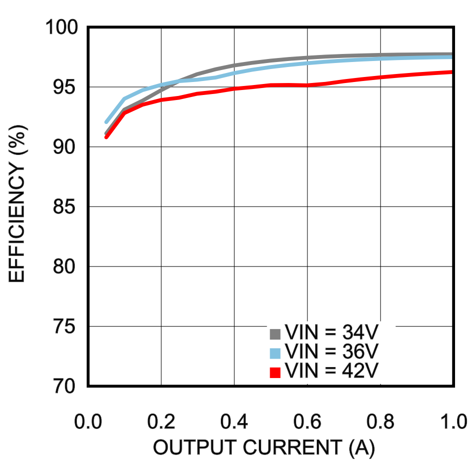
Efficiency V_{OUT} = 30V T_{AMB} = 25°C



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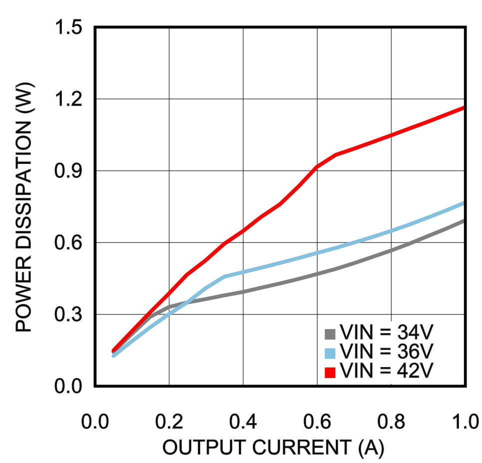
Power Dissipation V_{OUT} = 30V T_{AMB} = 25°C



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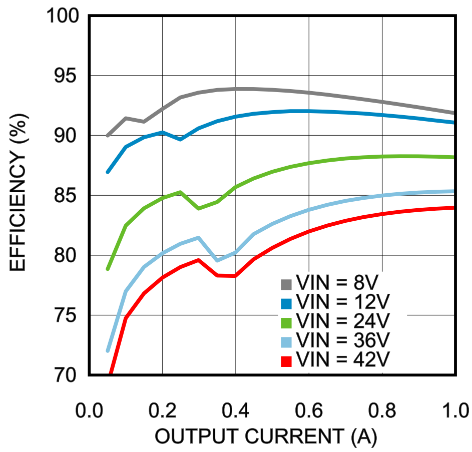
Efficiency V_{OUT} = 5.0V T_{AMB} = 85°C



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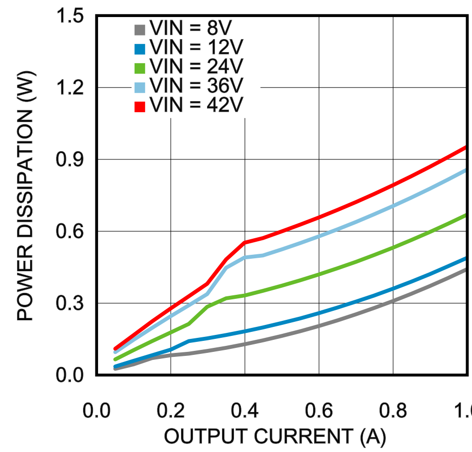
Power Dissipation V_{OUT} = 5.0V T_{AMB} = 85°C



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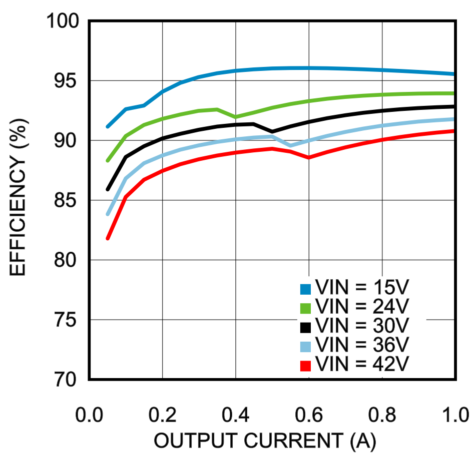
Efficiency V_{OUT} = 12V T_{AMB} = 85°C



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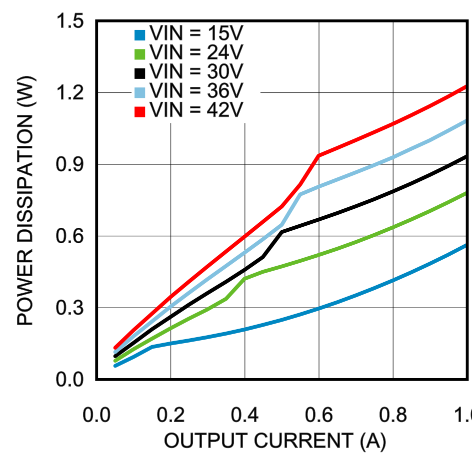
Power Dissipation V_{OUT} = 12V T_{AMB} = 85°C



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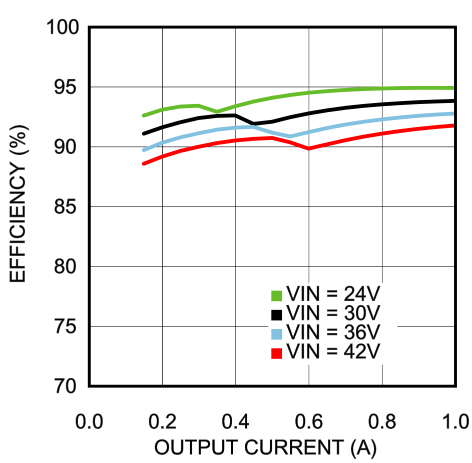
Efficiency V_{OUT} = 15V T_{AMB} = 85°C



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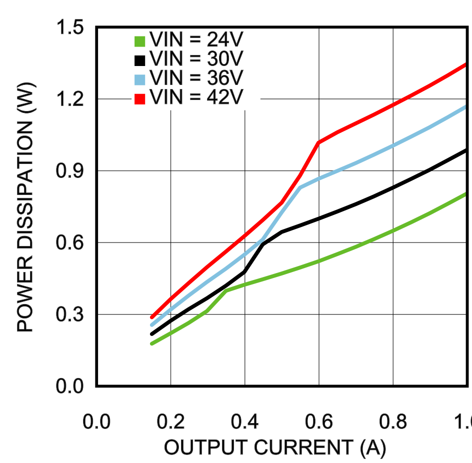
Power Dissipation V_{OUT} = 15V T_{AMB} = 85°C



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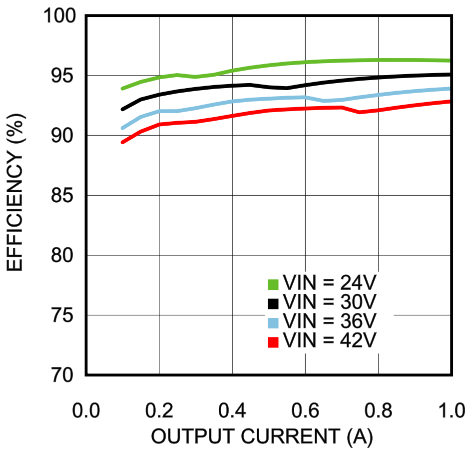
Efficiency V_{OUT} = 18V T_{AMB} = 85°C



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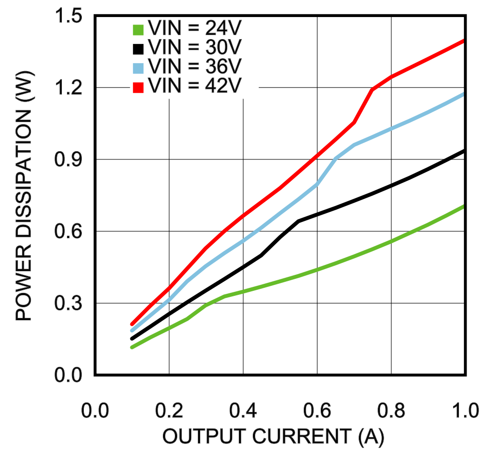
Power Dissipation V_{OUT} = 18V T_{AMB} = 85°C



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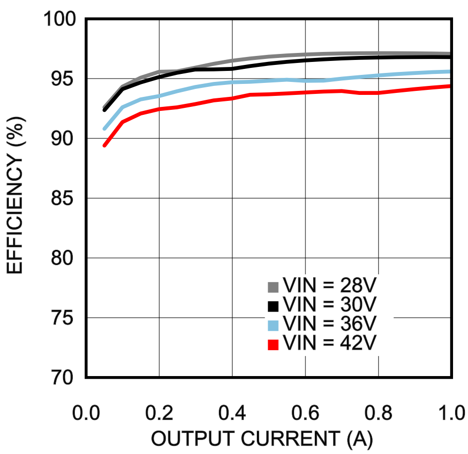
Efficiency V_{OUT} = 24V T_{AMB} = 85°C



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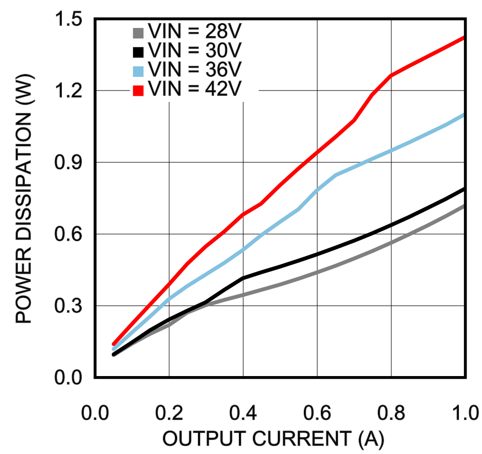
Power Dissipation V_{OUT} = 24V T_{AMB} = 85°C



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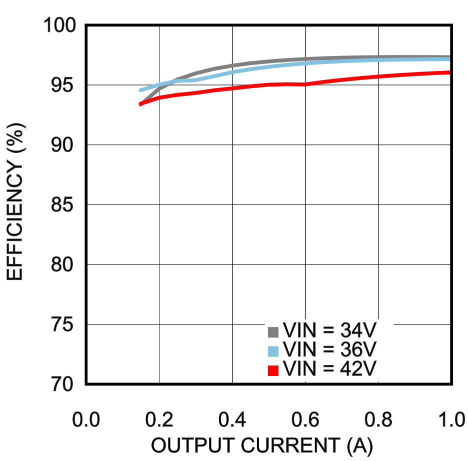
Efficiency V_{OUT} = 30V T_{AMB} = 85°C



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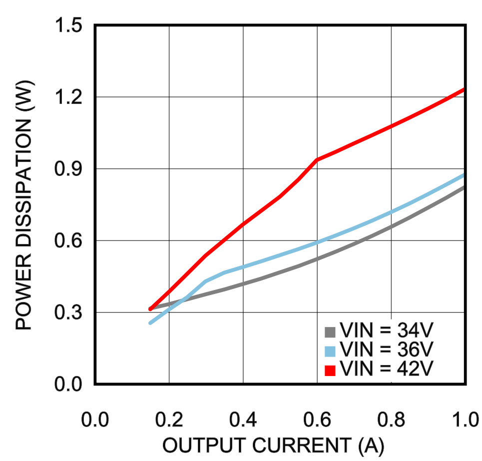
Power Dissipation V_{OUT} = 30V T_{AMB} = 85°C



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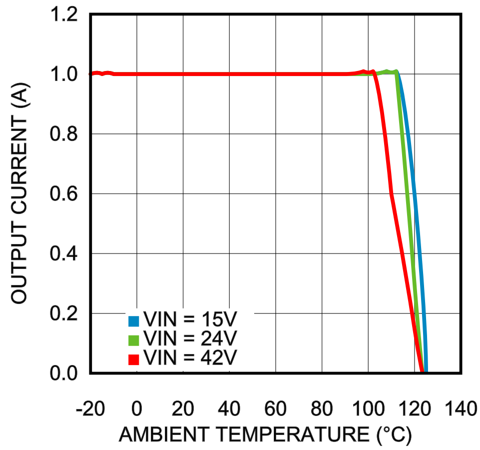
Thermal Derating V_{OUT} = 12V, θ_{JA} = 16°C/W



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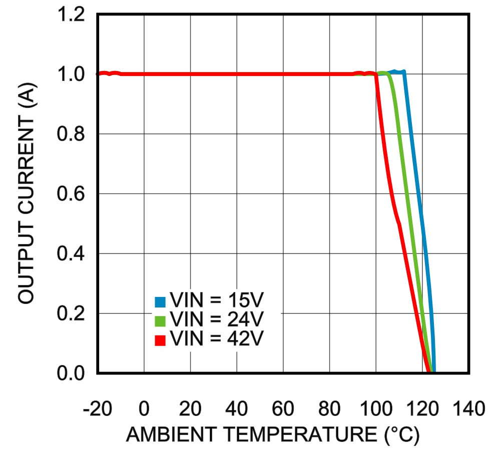
Thermal Derating V_{OUT} = 12V, θ_{JA} = 20°C/W



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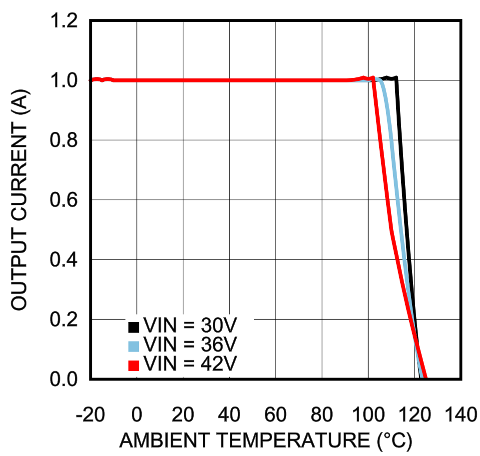
Thermal Derating V_{OUT} = 24V, θ_{JA} = 16°C/W



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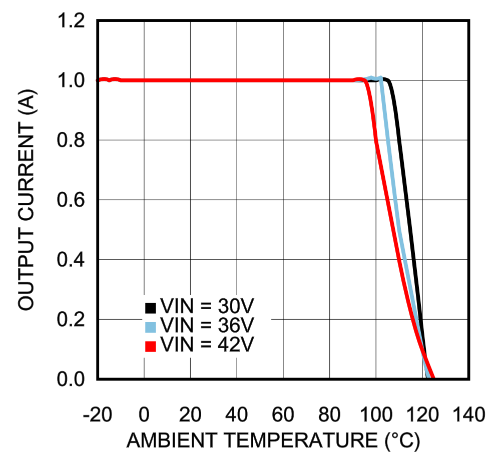
Thermal Derating V_{OUT} = 24V, θ_{JA} = 20°C/W



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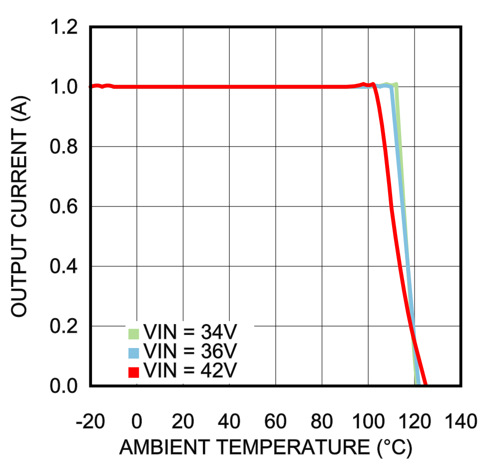
Thermal Derating V_{OUT} = 30V, θ_{JA} = 16°C/W



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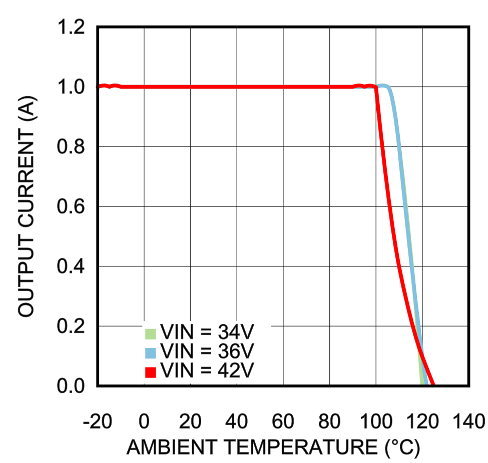
Thermal Derating V_{OUT} = 30V, θ_{JA} = 20°C/W



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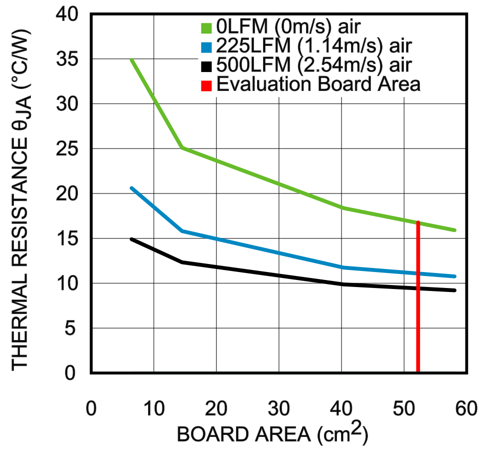
Package Thermal Resistance θ_{JA}
4 Layer Printed Circuit Board with 1oz Copper



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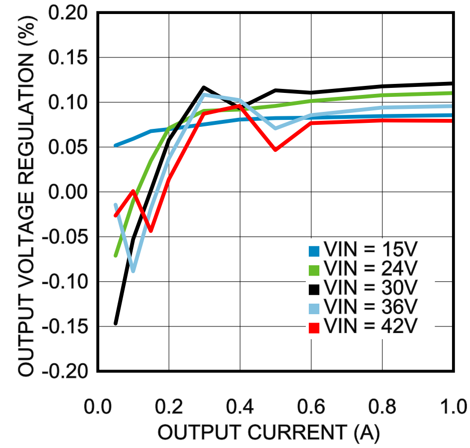
Line and Load Regulation T_{AMB} = 25°C



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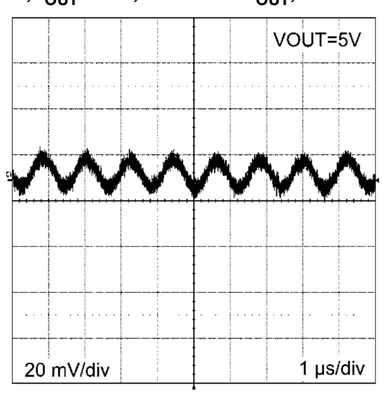
Output Ripple
V_{IN} = 12V, I_{OUT} = 1A, Ceramic C_{OUT}, BW = 200 MHz



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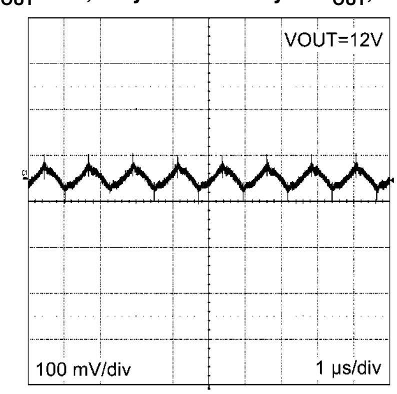
Output Ripple
V_{IN} = 24V, I_{OUT} = 1A, Polymer Electrolytic C_{OUT}, BW = 200 MHz



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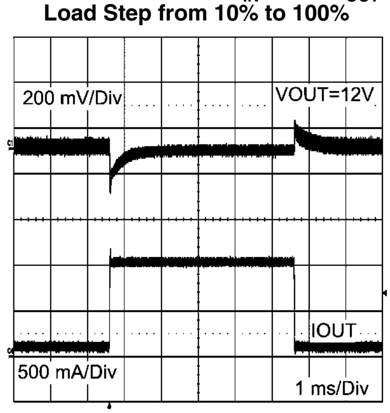
Load Transient Response V_{IN} = 24V V_{OUT} = 12V
Load Step from 10% to 100%



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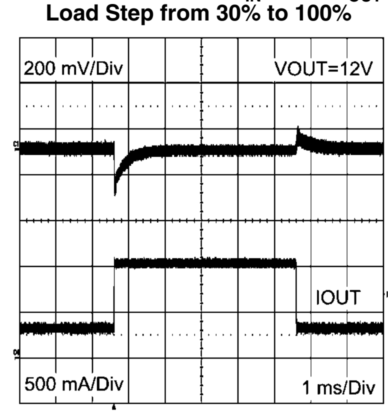
Load Transient Response V_{IN} = 24V V_{OUT} = 12V
Load Step from 30% to 100%



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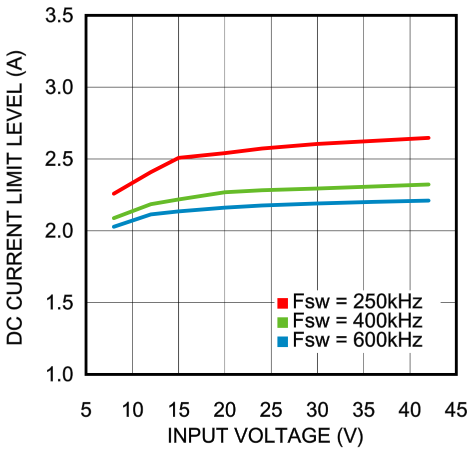
Current Limit vs. Input Voltage
V_{OUT} = 5V



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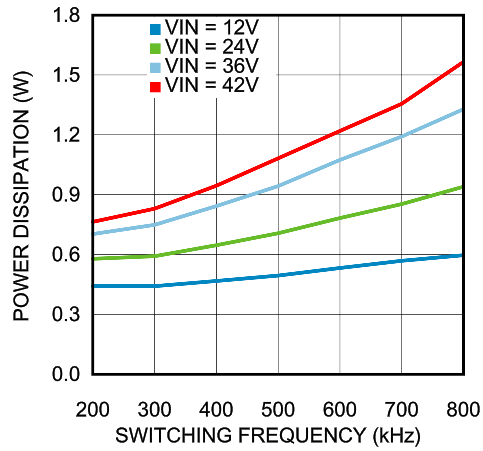
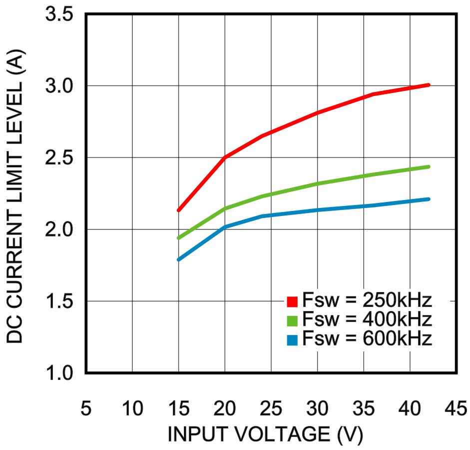
Switching Frequency vs. Power Dissipation
V_{OUT} = 5V



30135418

Current Limit vs. Input Voltage
V_{OUT} = 12V



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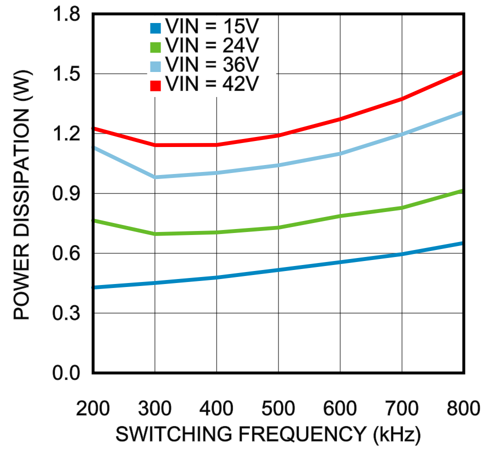
Switching Frequency vs. Power Dissipation
V_{OUT} = 12V



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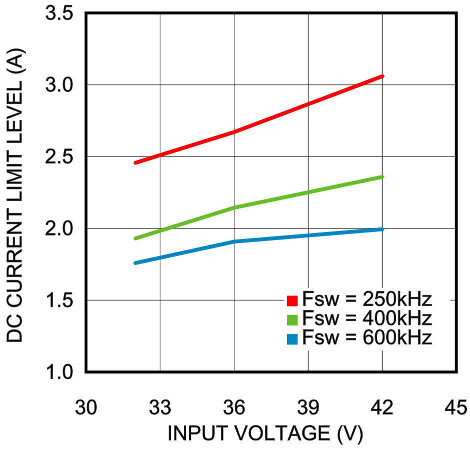
Current Limit vs. Input Voltage
V_{OUT} = 24V



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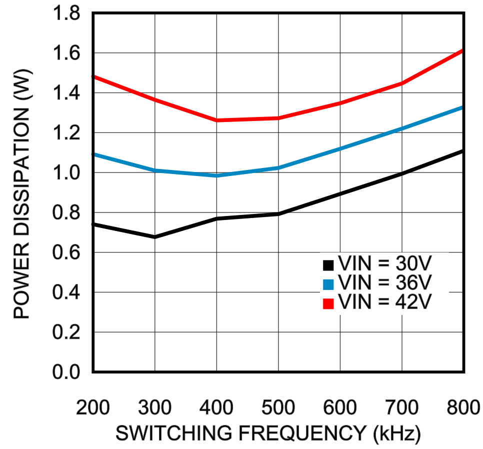
Switching Frequency vs. Power Dissipation
V_{OUT} = 24V



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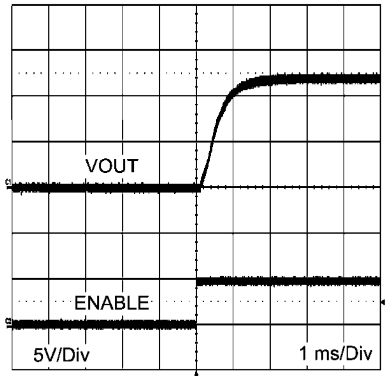
Startup
V_{IN} = 24V I_{OUT} = 1A



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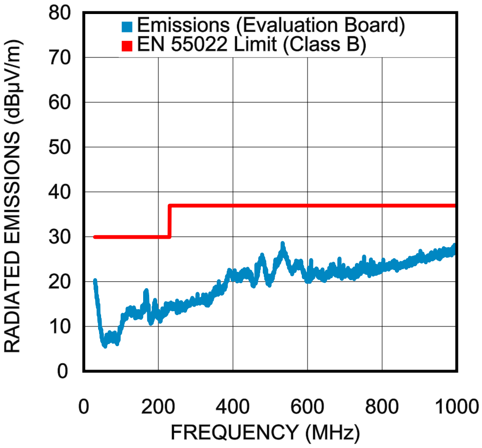
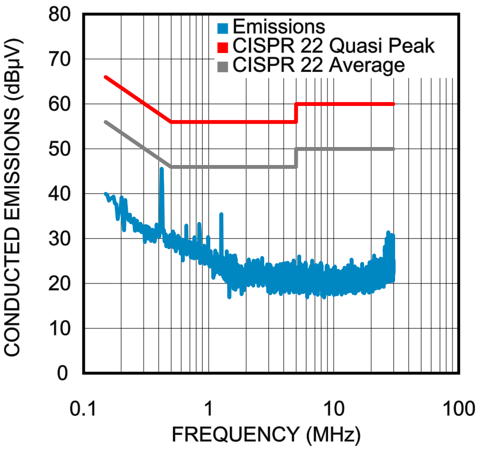
Radiated EMI of Evaluation Board, V_{OUT} = 12V



30135425

Conducted EMI, V_{OUT} = 12V
Evaluation Board BOM and 3.3µH 1µF LC line filter



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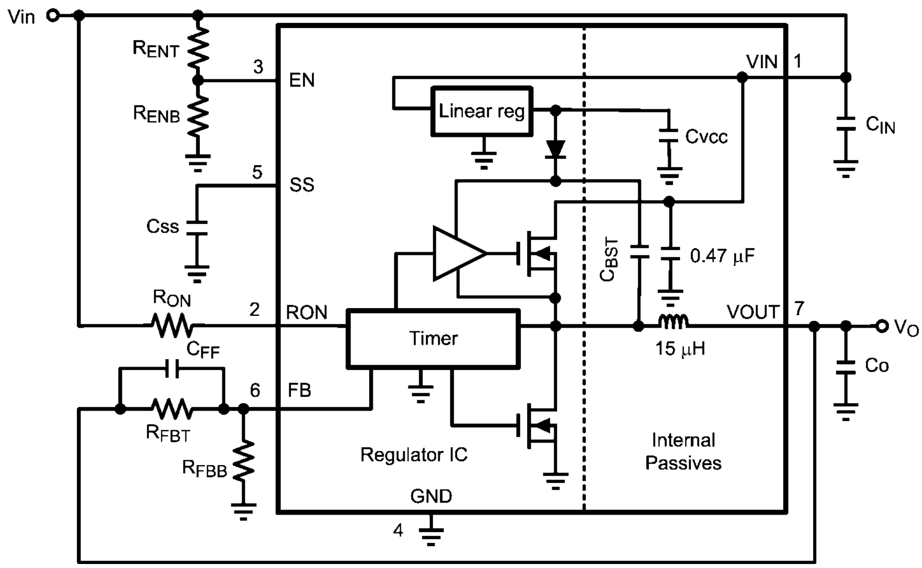
Application Block Diagram



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COT Control Circuit Overview

Constant On Time control is based on a comparator and an on-time one shot, with the output voltage feedback compared to an internal 0.8V reference. If the feedback voltage is below the reference, the high-side MOSFET is turned on for a fixed on-time determined by a programming resistor R_{ON}. R_{ON} is connected to V_{IN} such that on-time is reduced with increasing input supply voltage. Following this on-time, the high-side MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the on-time cycle is repeated. Regulation is achieved in this manner.

Design Steps for the LMZ14201H Application

The LMZ14201H is fully supported by Webench® which offers the following:

- Component selection
- Electrical simulation
- Thermal simulation
- Build-it prototype board for a reduction in design time

The following list of steps can be used to manually design the LMZ14201H application.

- Select minimum operating V_{IN} with enable divider resistors
- Program V_O with divider resistor selection
- Program turn-on time with soft-start capacitor selection
- Select C_O
- Select C_{IN}
- Set operating frequency with R_{ON}
- Determine module dissipation
- Layout PCB for required thermal performance

ENABLE DIVIDER, R_{ENT} AND R_{ENB} SELECTION

The enable input provides a precise 1.18V reference threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90 mV (typ) of hysteresis resulting in a falling threshold of 1.09V. The maximum recommended voltage into the EN pin is 6.5V. For applications where the midpoint of the enable divider exceeds 6.5V, a small zener can be added to limit this voltage.

The function of the R_{ENT} and R_{ENB} divider shown in the Application Block Diagram is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable under voltage lockout. This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turn-on of the supply as the main input voltage rail rises at power-up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14201H output rail. The two resistors should be chosen based on the following ratio:

$R_{ENT} / R_{ENB} = (V_{IN\text{-}ENABLE} / 1.18V) – 1$ ***(1)***

The EN pin is internally pulled up to VIN and can be left floating for always-on operation. However, it is good practice to use the enable divider and turn on the regulator when V_{IN} is close to reaching its nominal value. This will guarantee smooth startup and will prevent overloading the input supply.

OUTPUT VOLTAGE SELECTION

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8V internal reference. In normal operation an on-time cycle is initiated when the voltage on the FB pin falls below 0.8V. The high-side MOSFET on-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8V. As long as the voltage at FB is above 0.8V, on-time cycles will not occur.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$V_O = 0.8V \times (1 + R_{FBT} / R_{FBB})$ ***(2)***

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$R_{FBT} / R_{FBB} = (V_O / 0.8V) - 1$***(3)***

These resistors should be chosen from values in the range of 1 kΩ to 50 kΩ.

A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

A table of values for R_{FBT} , R_{FBB} , and R_{ON} is included in the simplified applications schematic.

SOFT-START CAPACITOR, C_{SS}, SELECTION

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

Upon turn-on, after all UVLO conditions have been passed, an internal 8uA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady state operation is given by the formula:

$t_{SS} = V_{REF} \times C_{SS} / Iss = 0.8V \times C_{SS} / 8uA$ ***(4)***

This equation can be rearranged as follows:

$C_{SS} = t_{SS} \times 8\ \mu A / 0.8V$ ***(5)***

Use of a 4700pF capacitor results in 0.5ms soft-start duration. This is a recommended value. Note that high values of C_{SS} capacitance will cause more output voltage droop when a load transient goes across the DCM-CCM boundary. Use equation 18 below to find the DCM-CCM boundary load current for the specific operating condition. If a fast load transient response is desired for steps between DCM and CCM mode the softstart capacitor value should be less than 0.018µF.

Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200 µA current sink:

- The enable input being “pulled low”
- Thermal shutdown condition
- Over-current fault
- Internal V_{IN} UVLO

OUTPUT CAPACITOR, C_O, SELECTION

None of the required output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst case RMS current rating of 0.5 x $I_{LR\ P\text{-}P}$, as calculated in equation (19). Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Low ESR capacitors, such as ceramic and polymer electrolytic capacitors are recommended.

CAPACITANCE:

The following equation provides a good first pass approximation of C_O for load transient requirements:

$C_O \geq I_{STEP} \times V_{FB} \times L \times V_{IN} / (4 \times V_O \times (V_{IN} - V_O) \times V_{OUT\text{-}TRAN})$***(6)***

As an example, for 1A load step, V_{IN} = 24V, V_{OUT} = 12V, $V_{OUT\text{-}TRAN}$ = 50mV:

$C_O \geq 1A \times 0.8V \times 15\mu H \times 24V / (4 \times 12V \times (24V - 12V) \times 50mV)$

$C_O \geq 10.05\mu F$

ESR:

The ESR of the output capacitor affects the output voltage ripple. High ESR will result in larger V_{OUT} peak-to-peak ripple voltage. Furthermore, high output voltage ripple caused by excessive ESR can trigger the over-voltage protection monitored at the FB pin. The ESR should be chosen to satisfy the maximum desired V_{OUT} peak-to-peak ripple voltage and to avoid over-voltage protection during normal operation. The following equations can be used:

$ESR_{MAX\text{-}RIPPLE} \leq V_{OUT\text{-}RIPPLE} / I_{LR\ P\text{-}P}$***(7)***

where $I_{LR\ P\text{-}P}$ is calculated using equation (19) below.

$ESR_{MAX\text{-}OVP} < (V_{FB\text{-}OVP} - V_{FB}) / (I_{LR\ P\text{-}P} \times A_{FB})$***(8)***

where A_{FB} is the gain of the feedback network from V_{OUT} to V_{FB} at the switching frequency.

As worst case, assume the gain of A_{FB} with the C_{FF} capacitor at the switching frequency is 1.

The selected capacitor should have sufficient voltage and RMS current rating. The RMS current through the output capacitor is:

$I(C_{OUT(RMS)}) = I_{LR\ P\text{-}P} / \sqrt{12}$ ***(9)***

INPUT CAPACITOR, C_{IN}, SELECTION

The LMZ14201H module contains an internal 0.47 µF input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance should be located as close as possible to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst case input ripple current rating is dictated by the equation:

$I(C_{IN(RMS)}) \cong 1 / 2 \times I_O \times \sqrt{(D / 1\text{-}D)}$ ***(10)***

where $D \cong V_O / V_{IN}$

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_O$).

Recommended minimum input capacitance is 10uF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature deratings of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain maximum value of input ripple voltage ΔV_{IN} to be maintained then the following equation may be used.

$C_{IN} \geq I_O \times D \times (1–D) / f_{SW\text{-}CCM} \times \Delta V_{IN}$***(11)***

If ΔV_{IN} is 1% of V_{IN} for a 24V input to 12V output application this equals 240 mV and f_{SW} = 400 kHz.

$C_{IN} \geq$ 1A x 12V/24V x (1– 12V/24V) / (400000 x 0.240 V)

$C_{IN} \geq$ 2.6µF

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

ON TIME, R_{ON}, RESISTOR SELECTION

Many designs will begin with a desired switching frequency in mind. As seen in the Typical Performance Characteristics section, the best efficiency is achieved in the 300kHz-400kHz switching frequency range. The following equation can be used to calculate the R_{ON} value.

$f_{SW(CCM)} \cong V_O / (1.3 \times 10^{-10} \times R_{ON})$ ***(12)***

This can be rearranged as

$R_{ON} \cong V_O / (1.3 \times 10^{-10} \times f_{SW(CCM)}$ ***(13)***

The selection of R_{ON} and $f_{SW(CCM)}$ must be confined by limitations in the on-time and off-time for the COT control section.

The on-time of the LMZ14201H timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$t_{ON} = (1.3 \times 10^{-10} \times R_{ON}) / V_{IN}$ ***(14)***

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the on-time at maximum V_{IN} is greater than 150 ns. The on-timer has a limiter to ensure a minimum of 150 ns for t_{ON}. This limits the maximum operating frequency, which is governed by the following equation:

$f_{SW(MAX)} = V_O / (V_{IN(MAX)} \times 150\ \text{nsec})$ ***(15)***

This equation can be used to select R_{ON} if a certain operating frequency is desired so long as the minimum on-time of 150 ns is observed. The limit for R_{ON} can be calculated as follows:

$R_{ON} \geq V_{IN(MAX)} \times 150\ \text{nsec} / (1.3 \times 10^{-10})$ ***(16)***

If R_{ON} calculated in (13) is less than the minimum value determined in (16) a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged.

Additionally, the minimum off-time of 260 ns (typ) limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

Discontinuous Conduction and Continuous Conduction Modes

At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the off-time. Note that during the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next on-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained since conduction and switching losses are reduced with the smaller load and lower switching frequency. Operating frequency in DCM can be calculated as follows:

$f_{SW(DCM)} \cong V_O \times (V_{IN}\text{-}1) \times 15\mu H \times 1.18 \times 10^{20} \times I_O / (V_{IN}–V_O) \times R_{ON}^2$ ***(17)***

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the off-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using equation 12 above.

The approximate formula for determining the DCM/CCM boundary is as follows:

$I_{DCB} \cong V_O x\ (V_{IN}–V_O)\ /\ (\ 2\ x\ 15µH\ x\ f_{SW(CCM)}\ x\ V_{IN})$ ***(18)***

The inductor internal to the module is 15µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$I_{LR\ P\text{-}P} = V_O\ x\ (V_{IN}\text{-}\ V_O)\ /\ (15µH\ x\ f_{SW}\ x\ V_{IN})$ ***(19)***

Where V_{IN} is the maximum input voltage and f_{SW} is determined from equation 12.

If the output current I_O is determined by assuming that $I_O = I_L$, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

POWER DISSIPATION AND BOARD THERMAL REQUIREMENTS

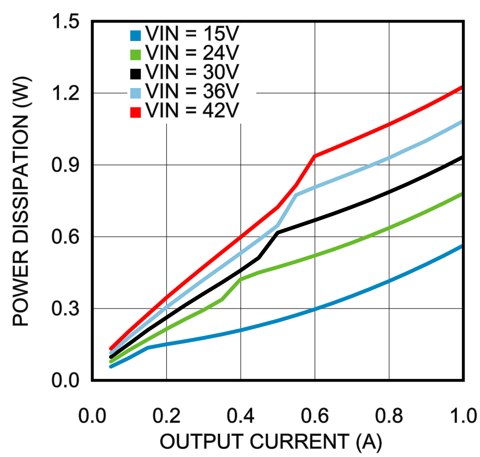
For a design case of V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 1A, T_{AMB} (MAX) = 85°C , and $T_{JUNCTION}$ = 125°C, the device must see a maximum junction-to-ambient thermal resistance of:

$\theta_{JA\text{-}MAX} < (T_{J\text{-}MAX}\ \text{-}\ T_{AMB(MAX)})\ /\ P_D$

This $\theta_{JA\text{-}MAX}$ will ensure that the junction temperature of the regulator does not exceed $T_{J\text{-}MAX}$ in the particular application ambient temperature.

To calculate the required $\theta_{JA\text{-}MAX}$ we need to get an estimate for the power losses in the IC. The following graph is taken form the Typical Performance Characteristics section and shows the power dissipation of the LMZ14201H for V_{OUT} = 12V at 85°C T_{AMB}.

Power Dissipation V_{OUT} = 12V T_{AMB} = 85°C



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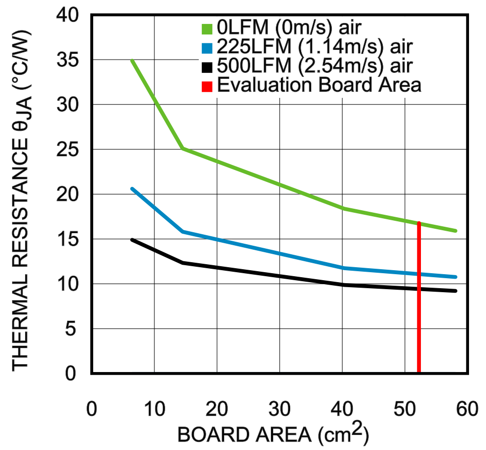
Using the 85°C T_{AMB} power dissipation data as a conservative starting point, the power dissipation P_D for V_{IN} = 24V and V_{OUT} = 12V is estimated to be 0.75W. The necessary $\theta_{JA\text{-}MAX}$ can now be calculated.

$\theta_{JA\text{-}MAX} < (125°C\ \text{-}\ 85°C)\ /\ 0.75W$

$\theta_{JA\text{-}MAX} < 53.3°C/W$

To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance. In order to estimate the necessary copper area we can refer to the following Package Thermal Resistance graph. This graph is taken from the Typical Performance Characteristics section and shows how the θ_{JA} varies with the PCB area.

Package Thermal Resistance θ_{JA} 4 Layer Printed Circuit Board with 1oz Copper



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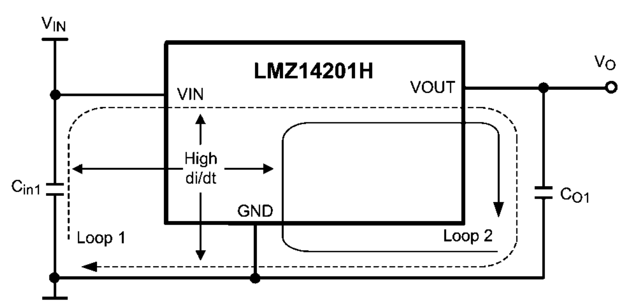
For $\theta_{JA\text{-}MAX}$< 53.3°C/W and only natural convection (i.e. no air flow), the PCB area can be smaller than 9cm^2. This corresponds to a square board with 3cm x 3cm (1.18in x 1.18in) copper area, 4 layers, and 1oz copper thickness. Higher copper thickness will further improve the overall thermal performance. Note that thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

For more guidelines and insight on PCB copper area, thermal vias placement, and general thermal design practices please refer to Application Note AN-2020 (http://www.national.com/an/AN/AN-2020.pdf).

PC BOARD LAYOUT GUIDELINES

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.



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1. Minimize area of switched current loops.

From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PC board layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (Cin1) is placed at a distance away from the LMZ14201H. Therefore place C_{IN1} as close as possible to the LMZ14201H VIN and GND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).

2. Have a single point ground.

The ground connections for the feedback, soft-start, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. Minimize trace length to the FB pin.

Both feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the LMZ14201H to minimize noise pickup.

4. Make input and output bus connections as wide as possible.

This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. Provide adequate device heat-sinking.

Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 x 6 via array with minimum via diameter of 10mils (254 μm) thermal vias spaced 59mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

Additional Features

OUTPUT OVER-VOLTAGE COMPARATOR

The voltage at FB is compared to a 0.92V internal reference. If FB rises above 0.92V the on-time is immediately terminated. This condition is known as over-voltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET on-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

CURRENT LIMIT

Current limit detection is carried out during the off-time by monitoring the current in the synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds the I_{CL} value, the current limit comparator disables the start of the next on-time period. The next switching cycle will occur only if the FB input is less than 0.8V and the inductor current has decreased below I_{CL}. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds I_{CL}, further on-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer off-time. It should also be noted that DC current limit varies with duty cycle, switching frequency, and temperature.

THERMAL PROTECTION

The junction temperature of the LMZ14201H should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typ) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145 °C (typ Hyst = 20 °C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

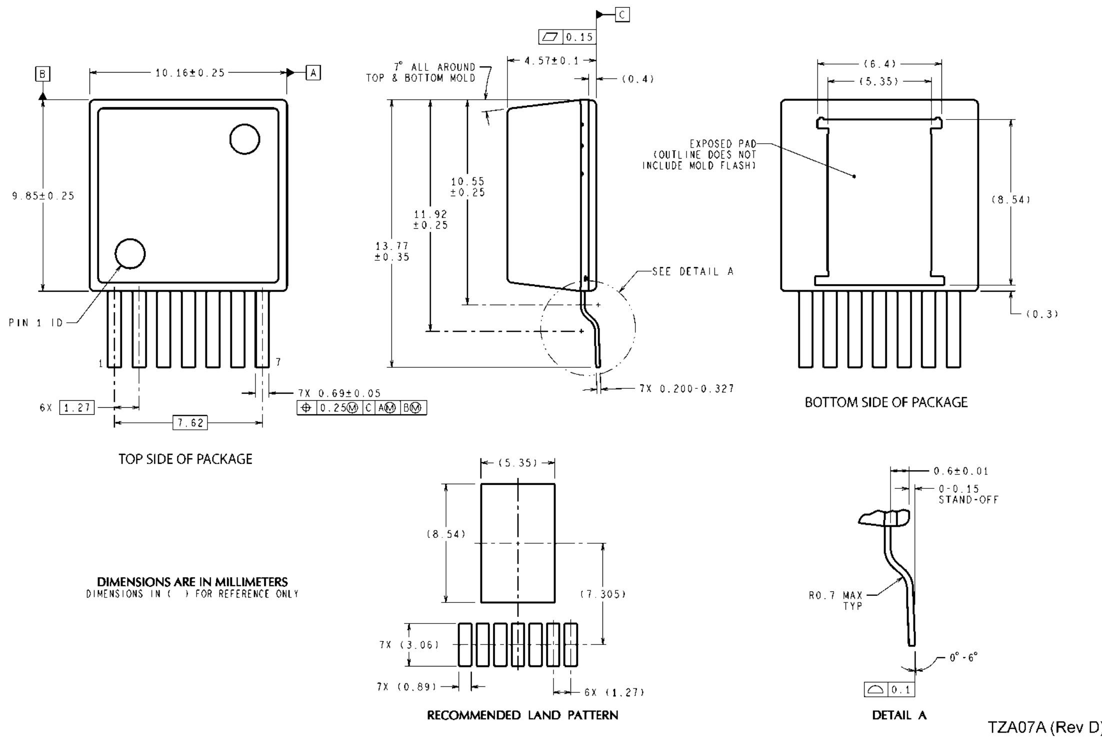
ZERO COIL CURRENT DETECTION

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next on-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

PRE-BIASED STARTUP

The LMZ14201H will properly start up into a pre-biased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The pre-bias level of the output voltage must be less than the input UVLO set point. This will prevent the output pre-bias from enabling the regulator through the high side MOSFET body diode.

Physical Dimensions inches (millimeters) unless otherwise noted



7-Lead TZA Package
NS Package Number TZA07A

Notes

Notes

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

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